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Neuromorhic Silicon Neuron and Synapse: Analog VLSI Implemetation of Biological Structures

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ABSTRACT
Neuromorphic Silicon neurons and synapses are very large scale integration (VLSI) circuits that emulate or mimic the electrophysiological behavior of their biological counterparts. These analog circuits can be used for the qualitative analysis of the functioning of neural circuits; and also for making intelligent systems that can perform the tasks that can be easily performed by biolological organisms but are very difficult to be performed by any traditionally engineered systems. Here we describe the analog very large-scale integration (aVLSI) realisation of integrate-and-fire neuron models and also discuss about plastic and non-plastic silicon synapses briefly.
Keywords **-** analog VLSI, integrate and fire, neuromorphic, plastic, subthreshold, silicon neuron, silicon synapse.

I. INTRODUCTION

Biological information processing systems are compact, energy efficient and excel at sensory perception, classification, association and control – areas in which modern digital computers falter. In order to study the nervous system a reasonable starting point is to model its basic units, neurons and synapses, thus developing biologically-inspired hardware systems.

It was first observed by Carver Mead that the CMOS circuits operating in the sub-threshold region have current–voltage characteristics similar to that of ion-channels present in neurons and also consume less power; hence can used as analogues of neuron. This observation of CMOS transistor physics led to the development of neuromorphic silicon neurons. These neurons permit neural spiking features to be emulated directly on analog VLSI chips without performing any digital software simulation.[1] They are much more energy efficient than simulations performed by general purpose computers, thereby making them suitable for real-time large-scale neural emulations.

These typically analog circuits exploit the inherent physics of transistors to produce an efficient computation of a particular task. To the extent that the physics of the transistors matches well the computation to be performed, the analog VLSI circuits use less power and silicon area than would an equivalent digital system. This is an important advantage because any serious attempt to replicate the computational power of brains must use resources as effectively as possible. The brain performs about 10^{15} operations per second.

Using the best digital technology that can be envisaged, this performance would dissipate over 10 MW, by comparison with the brain's consumption of only a few Watts. Neuromorphic analog VLSI circuits are also no match for neuronal circuits, but they can be a factor of 10^4 more power efficient than their digital counterparts. Another advantage is scaling capability of VLSI circuits which enables these circuits to operate efficiently without considering size of the network. But these silicon neurons only provide qualitative analysis of the performance and are not suitable for detailed quantitative approximations which can be done easily by digital simulation.

Real neurons have a complex morphology and even more complex biophysics, whose full emulation is beyond the reach of present electronic technology. The first artificial neuron model was proposed in the 1943 by McCulloch and Pitts. Hardware implementations of this model date almost back to the same period. Hardware implementations of spiking neurons are relatively new. But this sort of implementation of neuron model like Hodgkin-Huxley is not possible as it requires large amount of chip area and is also not affordable in terms of the required computational resources. Therefore, other simplified model, such as integrate and fire (IF) or leaky integrate and fire (LIF), which is a bold simplification of real neurons, has proved to have significant explanatory power in understanding the behavior of neuronal networks both in theory and

simulation. So far, it is this simplified model that has received the most attention in neuromorphic circles.

II. VLSI SUBTHRESHOLD MOS TECHNOLOGY

In sub-threshold region MOS transistors have their gate-to source voltage below the transistor threshold voltage Vth. Under these conditions, very low value (typically of the order of nanoamperes) of currents flow through the source and drain terminals of the transistor. The exponential increase in the transistor current with gate voltage (Fig. 1) can be used to make analog circuits with exponential and logarithmic properties that are useful for emulating neural properties. [2, 3]

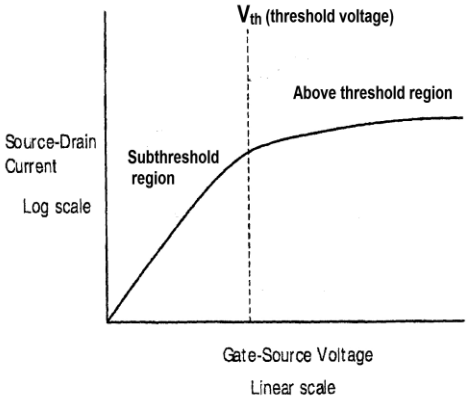


Fig 1: Current I_{ds} as a function of gate-to-source voltage V_{gs}

III. INTEGRATE-AND-FIRE (I&F) NEURON MODELS IN SILICON

The integrate-and-fire neuron model (also known as threshold fire model) is one of the most widely used models. It captures the notion of the membrane being charged by currents flowing into it and, upon the membrane potential exceeding a threshold, generating an action potential and discharging. These neurons are a particular case of simplified models that derived from the pioneering work of the French physiologist Louis Lapicque (1907).

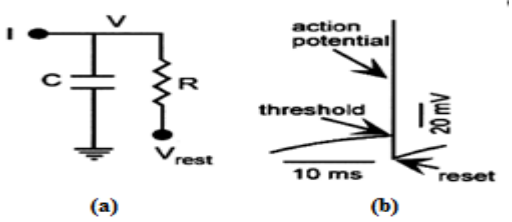


Fig 2: The integrate-and-fire model of Lapicque.

(a) The equivalent circuit (b) The voltage trajectory of the model.

He put forward a model of the neuron membrane potential (Fig. 2) in terms of an electric circuit consisting of a resistor and capacitor connected in parallel, that represented the leakage and capacitance of the nerve cell membrane.

Fig. 2(a) shows the equivalent circuit with membrane capacitance C and membrane resistance R. V is the membrane potential, Vrest is the resting membrane potential, and I is injected current. Fig.2(b) shows the voltage trajectory of the model.[4] When potential V reaches a threshold value, then an action potential is generated and V is reset to a sub-threshold value. In this model the membrane capacitor is charged until it reaches a certain threshold, at which time it discharges, producing an action potential (spike) and the potential is reset. Thus the traditional form of an integrate-and-fire model has sub-threshold integration domain (where the neuron integrates the inputs I(t)) and a threshold voltage for the generation of action potential.

The biological neuron membrane is assumed to be leaky due to the presence of ion channels, and as a consequence, the membrane potential has a tendency to decay back towards its resting value. When the membrane potential reaches a (fixed) threshold, an output spike is generated–the integrate-and-fire mechanism. After the membrane potential crosses threshold it is reset to its resting value and is inactivated for a brief time corresponding to the refractory period of the neuron. The basic model is therefore also called as leaky-integrate-and-fire (LIF) neuron model.

I&F neurons integrate pre-synaptic input currents and generate a voltage pulse analogous to an action potential when the integrated voltage reaches a spiking threshold. A number of VLSI networks of integrate–and–fire (I&F) neurons have been developed. Some of these implementations are discussed in the following sub-sections.

3.1 Axon-Hillock Circuit

The first simple VLSI version of integrate-and-fire neuron was probably the Axon-hillock circuit, that was proposed by Carver Mead and his colleagues in the late 1980s. In this circuit, a capacitor that represents the neuron's membrane capacitance (C_{mem}) integrates current input to the neuron. On the capacitor potential exceeding the spiking threshold, a pulse V_{out} is generated and the membrane potential V_{mem} is reset. This circuit captures the basic principle of operation of biological neurons, but is unable to match with the complete dynamics observed in real neurons. Fig.3 shows a schematic diagram of Axon-Hillock circuit.

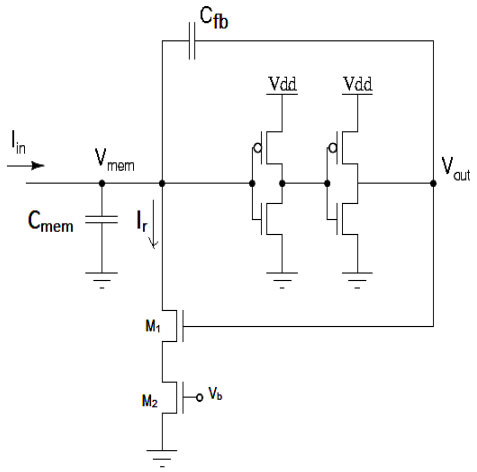


Fig 3: Schematic diagram of Axon-Hillock Integrate-and-Fire Circuit

The two inverters connected in series form the non-inverting amplifier. I_{in} is the synaptic current and V_{mem} is the neuron membrane potential. The resetting mechanism is implemented with the two transistors M_1 and M_2.the first one acts as a switch that activates when V_{out} goes high, while M_2 acts as the current controller and imposes the maximum value of current I_r (according to the bias V_b) and hence the duration of the spike pulse input currents.

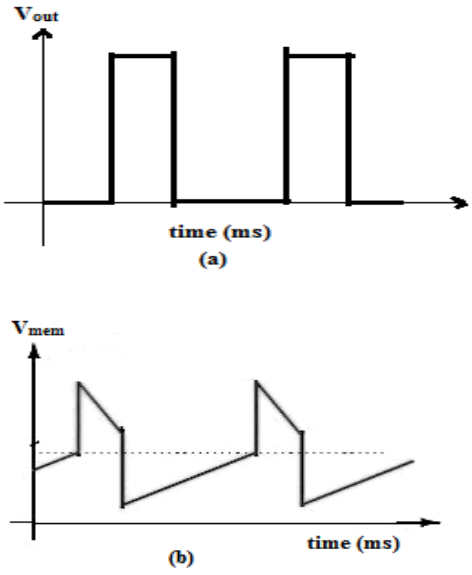


Fig 4: (a) Output voltage; (b) membrane voltage trace over time

The working of the circuit is as follows: input current I_{in} is integrated on the membrane input capacitance C_{mem}, and leading to the linear increase in the voltage V_{mem} until the amplifier switching threshold is attained. At this point Vout quickly changes from 0 to V_{DD} switching on the reset transistor M_1 and activating a positive feedback through the capacitor divider implemented by the feedback capacitor C_{fb} and C_{mem}. The membrane capacitor is discharged, if the reset current I_r set by V_b is larger than the input current, the discharging continues till the amplifier's switching threshold is retained. At this point V_{out} swings back to 0 and the cycle repeats. The transition in the voltage levels of V_{out} with respect V_{mem} is shown in Fig. 4(a) and the trace for membrane voltage V_{mem} over time is shown in Fig. 4(b).

The Axon-Hillock circuit is very compact and allows for implementations of dense arrays of silicon neurons. It has a major drawback: it dissipates non-negligible amounts of power. This is is due to the fact that the input to the inverter (the voltage on the capacitor) changes typically with time constants of the order of milliseconds, and the inverter spends a large amount of time in the region in which both transistors conduct a short-circuit current. A further drawback is that the Axon–Hillock circuit has a spiking threshold that depends only on CMOS process parameters (the switching threshold of the inverter), and does not model additional neural characteristics, such as refractory period mechanisms. [5]

3.2 Voltage-Amplifier Integrate-and-Fire Neuron

In order to have better control over the spiking threshold, a very simple neuron model was developed by van Schaik in 2001 [6]. The schematic diagram of this neuron model is shown in Fig. 5(a). This neuron circuit comprises circuits for both setting explicit spiking thresholds and implementing an explicit refractory period. This circuit uses an amplifier at the input, for comparing the capacitor voltage with a desired spiking threshold voltage. When the input exceeds the threshold, the amplifier runs the inverter, making its switching very fast.

Fig. 5(b) shows various stages that involve membrane potential V_{mem} in the process of generation of an action potential. The capacitance C_{mem} of this circuit works as the biological neuron membrane, while the controlling of the membrane leakage current is done by the gate voltage V_{lk}, of an nMOS.

In the absence of any input the membrane voltage will be drawn to its resting potential (ground, in this case), by this leakage current. Excitatory inputs (e.g., modeled by I_{in}) add charge to the membrane capacitance, whereas charge is removed from the membrane capacitance by the inhibitory inputs (not shown). On applying an excitatory current that is larger than the leakage current, there will be an increase in the membrane potential V_{mem} from its resting potential. Comparision of this membrane potential V_{mem} with the controllable threshold voltage

V_{thr} is done with the help of a basic transconductance amplifier. If V_{mem} exceeds V_{thr}, an action potential is generated which is similar to the process occurring in the biological neuron, where an increased level of sodium conductance leads to the rising edge (depolarizing phase) of the spike, and a delayed increased level of the potassium conductance gives the falling edge (repolarising phase) of the spike.

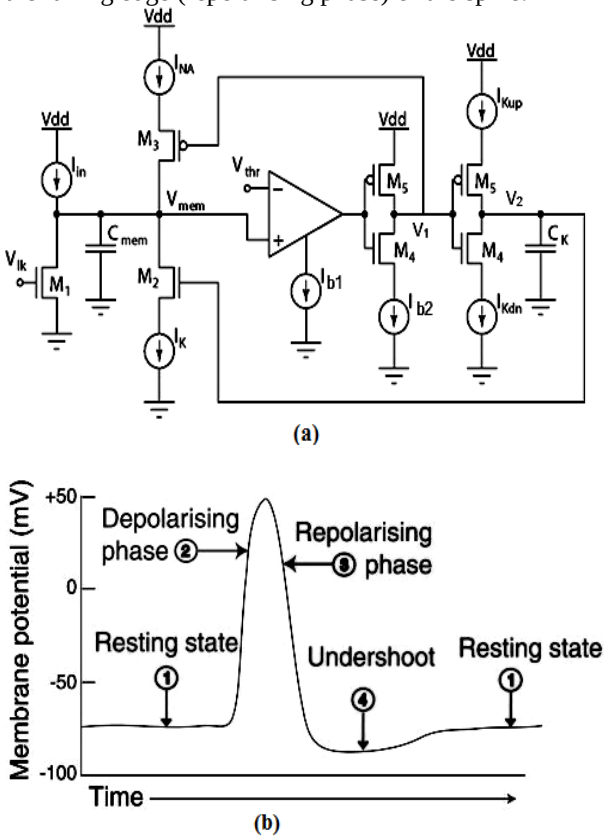


Fig 5: Voltage-amplifier I & F neuron
(a) Schematic Diagram; (b) Membrane voltage trace over time

In the circuit (Fig. 5a), this is modeled as follows: As V_{mem} rises above V_{thr}, the output voltage of the comparator will rise to the positive power supply. Thereby decreasing the output V_1 of the following inverter, and hence the sodium current I_{Na} pulls up the membrane potential. Simultaneously, second inverter allows the capacitance C_K to be charged at a speed which can be controlled by the current I_{Kup}. As soon as the voltage V_2 on capacitance C_K is high enough to cause conduction of the nMOS transistor M_2, the potassium current I_K will be able to discharge the membrane capacitance.

Two different potassium channel currents govern the opening and closing of the potassium channels: The current I_{Kup} that charges the capacitance C_K controls the spike width, as the delay between the opening of the sodium ion channels and the opening of the potassium ion channels is inversely proportional to the current I_{Kup}. If V_{mem} now drops below V_{thr}, the output of the first inverter V_1 will become high, cutting off the current I_{Na}. The second inverter then allows the capacitance C_K to be discharged by the current I_{Kdn}. If I_{Kdn} is small, the voltage on C_K decreases slowly, and, as long as this voltage remains high enough to permit the current I_K to discharge the membrane, it will not be possible to stimulate the neuron for I_{ex} values smaller than I_K. Therefore I_{Kdn} controls the refractory period of the neuron. Finally I_{b1} and I_{b2} are two bias currents needed to limit the power consumption of the circuit; they do not influence the spiking behaviour of the neuron.

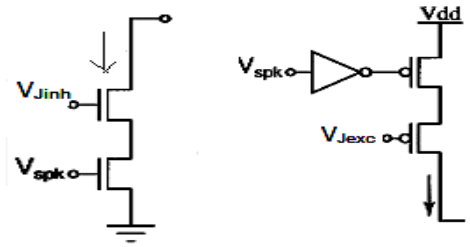
IV. SILICON SYNAPSES

To implement networks of integrate-and-fire neurons we can connect the circuits, described in section III, with each other with silicon synapses. These synapses can of two types depending on their efficacy: non-plastic (fixed) or plastic. Synapses can also be classified as excitatory or inhibitory. In the first case, given the silicon neuron, they source current into the neuron's membrane capacitor. In the second case they sink current from the neuron's membrane capacitor. Using excitatory and inhibitory synaptic circuits, interfaced to silicon neurons, it is possible to design neural networks of arbitrary complexity. The size of the silicon neural network is only limited by the chip's surface. Using a low-cost technology and small chip sizes, it is already possible to fabricate networks with thousands of neurons (and synapses).

4.1 Non-plastic Synapses

The non-plastic synapse (also called fixed synapse) is implemented with a circuit that injects a fix amount of charge in the postsynaptic membrane capacitance upon presentation of a presynaptic spike. On silicon a synapse with a fixed efficacy is a simple device composed of two MOSFETs, one acting as a digital switch, the other as a current regulator. It is a simple excitatory postsynaptic current or inhibitory postsynaptic current block with only one possible value for the output current.

The inhibitory non-plastic synapses (Fig. 6a) are made of n-type MOSFETs whose task is to suck current from the neuron capacitors upon the arrival of a presynaptic spike (V_{spk}). This has an inhibitory effect on the postsynaptic neuron because it induces a decrease in the voltage V_{mem} moving it away from the spike emission threshold. The inhibitory current is controlled by the bias voltage V_{Jinh}.



(a) (b)

Fig 6: Schematic Diagram of Non-Plastic Synapse
(a) Inhibitory Synapse; (b) Excitatory Synapse

The excitatory non-plastic synapses (Fig. 6b) are made of p-type MOSFETs. They work in an analogous way: when they receive active-low spikes from the presynaptic neuron, they inject current thus provoking upward jumps for the membrane potential V_{mem}. The excitatory post synaptic current is set by the bias voltage V_{Jexc}. The synaptic weight of these synapses can be set by changing the bias voltages V_{Jinh} and V_{Jexc}.[7]

4.2 Plastic Synapse

The ultimate aim of neuromorphic engineering is to mimic the capabilities of biological perception and information processing with a compact and energy-efficient platform. It is widely believed that this goal necessitates from the outset some mechanisms of learning that enables neuromorphic devices to adapt (or re-configure) themselves while interacting with an environment. Emulating the example of biological neurons and synapses, neuromorphic devices attain ability for learning by incorporating Hebbian-like mechanisms of synaptic plasticity.

In the Hebbian scenario, the efficacy of a synapse is enhanced (i.e., its impact on the post-synaptic neuron is increased), when both the pre- and postsynaptic neurons are simultaneously highly active on a suitable time-scale, and reduced if the pre-synaptic neuron is active while the post-synaptic is not.

A simple pulsed circuit explaining Hebb's Learning Rule is shown in Fig 7. Here V_{pre} and V_{post} represent the pre- and post-synaptic signals respectively. Whenever pre- and post-synaptic pulses occur together, the single MOSFET gate is pulsed and a small current carries charge onto the capacitor. [8]

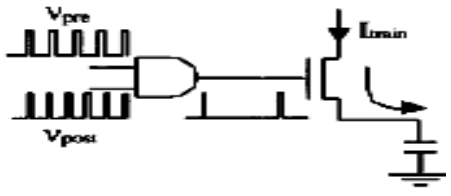


Fig 7: A simple pulsed circuit for Hebb's Rule

The excitatory neurons are connected by plastic synapses. These plastic synapses are much more complex than the non-plastic synapses. Their dynamics is described in terms of a single internal variable (V_{syn}), which represents the voltage across a capacitor. Even though V_{syn} is inherently analog in nature, the synapse is designed in such a way that only the maximum and the minimum allowable values of V_{syn} are stable on long time scales, in the absence of presynaptic neuronal activity. A positive current drives V_{syn} to the upper bound (V_{DD}) when voltage V_{syn} is above some threshold voltage V_{thr}; otherwise, the synaptic capacitor is discharged at a regular speed until the voltage V_{syn} meets the lower bound (0V). These two values are then preserved indefinitely and survive also in the presence of small fluctuations which do not bring V_{syn} across the threshold V_{thr}.

This bistability preserves the memory of one of the two states on long time scales and, hence, these two currents are referred to as the refresh currents. Arrival of a presynaptic spike,leads to modification of the internal state of the synapse in order to acquire information about the neuronal activity and, hence, about the stimulus. If the postsynaptic depolarization is above some threshold V_{ref}, the internal state V_{syn} is pushed upwards (synaptic potentiation); otherwise, it is pushed downwards (synaptic depression). If these temporary changes accumulate and bring Vsyn across the threshold V_{thr}, the synapse is then attracted toward a different stable state, and a transition occurs. The presynaptic activity acts as a trigger (no transition can occur in case of low presynaptic spike frequency) and, then, the direction of the change is determined by the depolarization of the postsynaptic neuron. [7]

V. CONCLUSION

Complementary metal oxide semiconductor (CMOS) very large scale integration (VLSI) technology is being used extensively to construct a wide range of neural analogs, from single synapses to networks of spiking neurons, and simple vision processing devices with the intention of emulating brain-like real-world behavior in hardware and robotic systems rather than simply simulating their performance on general-purpose digital computers.

A family of simpler spiking neuron models that permits the implementation of large, massively parallel networks in VLSI is the Integrate-and-fire neuron model and so its VLSI implementation was the prime focus of this paper. Different VLSI models like Axon-Hillock circuit, voltage-amplifier integrate-and-fire neuron were discussed. In addition to these neuron models, silicon synapse was also described.

Neuromorphic systems' implementations may take place at a number of different levels. For example, one may model sensory processing like that for vision, audition and other sensory modalities like olfaction (electronic nose used in brewing and perfumery industries) or sensorimotor systems, or one may model specific neural systems at many different levels, ranging through brain region, cortical column, mid-brain or brainstem nucleus, neural microcircuits, single neurons, structural parts of neurons (dendrites, axons, soma), patches of membrane, down to ion channels encased in the neural bilipid membrane.

There remains considerable interest in auditory and visual neuromorphic systems as technologies for eventually producing synthetic sensing systems with the same types of capabilities as biological auditory and visual systems. The rapid responses of the neuromorphic camera in without the use of large-scale frame technology represent a real step forward. Another area of progress is likely to be in the integration of different types of sensors on to CMOS systems. Light sensors have been around for a long time, and polymer based sensors are in use in olfactory neuromorphic systems.

Thus the silicon neuron models discussed in this paper and many others already developed or that are in the developing phase, that are the building blocks of the neuromorphic systems, help in testing various theories relating to the functioning of the nervous system; thus providing a better understanding of the biology and thus helping in the development of neural prostheses. In addition to this, robotic parts that emulate the nervous system can also be designed leading to more intelligent robots that will able to interact with their environment with limited human intervention.

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